REMARKS

The Examiner has objected to the drawings under 37 CFR 1.83a stating; "The drawings must show every feature of the invention. Therefore, a transistor.... comprising functional gate conductors (i.e. claim 1) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.. It appears (i.e. FIG. 1A) there are multiple transistors each having a single functional gate conductor, however, the figures do not show a single transistor which has multiple functional gate conductors.

Applicants have addressed this objection in Applicants traversal of the Examiners 35 U.S.C. 112 (second paragraph) rejections.

The Examiner rejected claims 1-22 and 30-33 under 35 U.S.C. 112 (second paragraph) "as being indefinite for failing to particularly point out and distinctly claim the subject mater which applicant regards as the invention."

The Examiner rejected claims 1,4-12, 15-22 under 35 U.S.C. §103(a) as being unpatentable over Iwasaki (US 6,833,595 in view of Uehara ET AL. (US 5,946,563).

The Examiner rejected claims 2, 3, 13 and 14 under 35 U.S.C. §103(a) as being unpatentable over Iwasaki in view of Uehara et al. in further view of Fukuda (US 6,660,462 B1).

The Examiner rejected claims 30-33 under 35 U.S.C. §103(a) as being unpatentable over Iwasaki in view of Uehara et al. in further view of Kang (US 6,872,990 B1).

Applicants respectfully traverse the 35 U.S.C. §112(second paragraph) rejections, drawing objections and 35 U.S.C. §103(a) rejections with the following arguments:

35 USC § 112 and Drawing Objections

As to claims 1 and 12, the Examiner states that "In claims 1, and 12, it is unclear how the applicant defines a transistor. From FIG. 1A, it appears that there are multiple transistors (each having a source and drain) that use a functional gate conductor, however, it is not a single transistor (i.e. "transistor in a substrate") that comprises functional gate conductors. Appropriate clarification and/or correction are required."

Applicants respectfully remind the Examiner that FIG. 1B is a cross-section through FIG. 1A and that in FIG. 1A all functional gate conductors 105 are integral with spine 110 and thus a single FET is illustrated in FIGs. 1A and 1B. Further, Applicants specification, on page 5, second full paragraph states: "Since all functional gate conductors **105** are integrally formed with spine **110**, a single FET is formed having a gate (or channel) length equal to L_{DES} and a gate (or channel) width equal to L_{DES} times the number of functional gate conductors **105**. In the example of FIG. 1A, there are 9 functional gate conductors **105** so the width of the single FET is $9W_{DES}$."

Based on the preceding arguments, Applicants respectfully maintain that there is no basis for the Examiners objection to drawing (FIG. 1A) or for the Examiners rejection of claims 1-22 and 30-33 under 35 U.S.C. §112(second paragraph) and respectfully request the Examiner withdraw the objection of drawing FIG. 1A and the rejection of claims 1-22 and 30-33 under 35 U.S.C. §112(second paragraph).

35 USC § 103 Rejections

As to claims 1 and 12, the Examiner states, in part "The dummy gates are not positioned between gates 1, 2 and adjacent to ends of said gates."

Applicants contend that claims 1 and 12 are not obvious in view of Iwasaki in view of Uehara in view of one of ordinary skill in the art does not teach or suggest every feature of claims 1 and 12. For example, Iwasaki in view of Uehara does not teach or suggest "said dummy gate conductors positioned adjacent to ends of said functional gate conductors."

First the Examiner appears to be saying that Iwasaki in view of Uehara is teaching that the dummy gates are not positioned adjacent to the ends of the functional gates whereas Applicants are claiming in Applicants claims 1 and 12 that "said dummy gate conductors" are " positioned adjacent to ends of said functional gate conductors."

Second, in FIG. 2, of Iwasaki, the source of the transistor intervenes between the ends of the dummy and functional gates so it is not possible in Iwaska for "said dummy gate conductors positioned adjacent to ends of said functional gate conductors" as Applicant claims 1 and 12 require.

Based on the preceding arguments, Applicants respectfully maintain that claims 1 and 12 are not unpatentable over Iwasaki in view of Uehara and are in condition for allowance. Since claims 2-11, 30 and 31 depend from claim 1 and claims 12-22. 32 and 33 depend from claim 12, Applicants respectfully maintain that claims 2-11, 12-22 and 30-34 are likewise in condition for allowance.

As to claims 7, 8, 18 and 19, the Examiner states "Iwasaki in view of Uehara does not disclose the length of said functional gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said

fixed distance, and the length of said dummy gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance. However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the length of said functional gate conductors and dummy gateconductors in order to minimize proximity effect, and improve manufacture of a semiconductor device. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the length of said functional gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance, and the length of said dummy gate conductors being a function of positive integer multiples of a minimum length of said gate conductors and of positive integer multiples of said fixed distance because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the length of said functional gate. conductors and dummy gate conductors in order to minimize proximity effect, and improve manufacture of a semiconductor device. See In re Aller, *105* USPQ 233."

Applicants contend that claims 7 and 13 are not obvious in view of Iwasaki in view of Uehara in view of one of ordinary skill in the art does not teach or suggest every feature of claims 7 and 13. For example, Iwasaki in view of Uehara in view of one of ordinary skill in the art does not teach or suggest "wherein the gate length of said **functional** gate conductors is a function of positive integer multiples of a minimum gate length of said **functional** gate conductors and of positive integer multiples of said fixed distance."

First, there is no mention of dummy gates in claims 7 and 13 which Applicants find confusing, as the Examiner appears to be arguing that varying functional gate length would be done to effect proximity correction of dummy gates, since it is impossible to vary the functional

gate length to effect proximity correction of the functional gate itself. Applicants most strongly contend, that no person of ordinary skill in the art would vary functional gate length to effect proximity correction of dummy gates.

Second, Applicants cite *In re Antonie*, 559 F.2d 618, 619, 195 U.S.P.Q. 6, 8 (C.C.P.A. 1977) which held that varying a variable to optimize a result is obvious only if the prior art has disclosed that the variable is a result effective variable for optimizing the result. All prior art cited by the Examiner have shown that dummy gate placement location and **dummy gate width** are the variables known to optimize the result "minimize(d) proximity effect, and improve(d) manufacture of a semiconductor device." Applicants know of no prior art, teaching that "**functional gate length**" will have any effect on, no less optimize the result "minimize(d) proximity effect, and improve(d) manufacture of a semiconductor device." There appears to be some confusion of "dummy" and "functional" and of "width" and "length."

Third, the Examiner has not provided any evidence from the prior art demonstrating that that a "positive integer multiple" relationship between " the gate length of said functional gate conductors" and "a minimum gate length" and "said fixed distance" between functional and dummy gate conductors is known in the prior art, no less would result in "minimize(d) proximity effect, and improve(d) manufacture of a semiconductor device."

Fourth, the Examiners statement " and improve manufacture of a semiconductor device" in ambiguous as the Examiner fails to show what in the "manufacture of a semiconductor device" is improved. Further, since the Examiners statement is so broad, Applicants contend that a person of ordinary skill in the art would not know what the Examiner believes was improved.

Based on the preceding arguments, Applicants respectfully maintain that claims 7 and 13, are not unpatentable over Iwasaki in view of Uchara in view of one of ordinary skill in the art and are allowable.

Applicants contend that claims 8 and 14 are not obvious in view of Iwasaki in view of Uehara in view of one of ordinary skill in the art does not teach or suggest every feature of claims 8 and 19. For example, Iwasaki in view of Uehara in view of one of ordinary skill in the art does not teach or suggest "wherein the gate length of said **dummy** gate conductors is a function of positive integer multiples of a minimum gate length of said **functional** gate conductors and of positive integer multiples of said fixed distance."

First, Applicants cite *In re Antonie*, 559 F.2d 618, 619, 195 U.S.P.Q. 6, 8 (C.C.P.A. 1977) which held that varying a variable to optimize a result is obvious only if the prior art has disclosed that the variable is a result effective variable for optimizing the result. All prior art cited by the Examiner have shown that dummy gate placement location and dummy gate **width** are the variables known to optimize the result "minimize(d) proximity effect, and improve(d) manufacture of a semiconductor device." Applicants know of no prior art, teaching that "dummy gate **length**" will have an effect on, no less optimize the result "minimize(d) proximity effect, and improve(d) manufacture of a semiconductor device. There appears to be some confusion of "width" and "length.

Second, the Examiner has not provided any evidence from the prior art demonstrating that that a "positive integer multiple" relationship between " the gate length of said dummy gate conductors" and "a minimum gate length" and "said fixed distance" between functional and dummy gate conductors is known in the prior art, no less would result in "minimize(d) proximity effect, and improve(d) manufacture of a semiconductor device."

Based on the preceding arguments, Applicants respectfully maintain that claims 8 and 14, are not unpatentable over Iwasaki in view of Uchara in view of one of ordinary skill in the art and are allowable.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0458.

Respectfully submitted,
FOR: Butt et al.

Dated: 09/19/2005

BY: Jack P. Friedman
Jack P. Friedman
Reg. No. 44,688
FOR:
Anthony M. Palagonia
Registration No.: 41,237

3 Lear Jet Lane, Suite 201
Schmeiser, Olsen & Watts
Latham, Previously Presented York 12110
(518) 220-1850
Agent Direct Dial Number: (802)-899-5460